Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults, wherein:

each of defined delay faults which are delay faults assumed to exist in a semiconductor integrated circuit is ~~weighted~~ assigned a predetermined delay value; and

~~a ratio~~ the result of the total of ~~the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to~~ the delay values of the "delay faults detected by the test sequences for delay faults" divided by the predetermined delay values of the defined delay faults is set as a fault coverage, thereby evaluating the quality of the "test sequences for delay faults".

4. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults including steps of:

~~weight~~ assigning a predetermined delay value to each of defined delay faults which are delay faults assumed to exist in a semiconductor integrated circuit;

determining a fault coverage by dividing the total of the delay values of the "delay faults detected by the test sequences for delay faults" by the total of the predetermined delay values of the defined delay faults ~~calculating a ratio of the total of the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to the defined delay faults as a fault coverage~~; and

evaluating the quality of the "test sequences for delay faults" based on the fault coverage.

5. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 3, wherein the result of a "design delay value on a signal path on which a delay fault is defined" divided by "timing design request value on the delay fault defined signal path" is used as the predetermined delay value ~~a relative value of a "design delay value on a signal path on which a delay fault is defined" with respect to a "timing design request value on the delay fault defined signal path" is used as the weight~~.

6. (Previously Presented)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 5, wherein a clock rate with respect to the delay fault defined signal path is used for the "timing design request value on the delay fault defined signal path".

7. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 3, wherein a "gate stage number with respect to the delay fault defined signal path" is used as the predetermined delay value ~~the weight~~.

8. (Currently Amended)   A method of evaluating the quality of test sequences for

delay faults as claimed in claim 3, wherein the product of the "design delay value on the delay fault defined signal path" and a "physical path length on the delay fault defined signal path" is used as <u>the predetermined delay value</u> ~~the weight~~.

9. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 3, wherein the product of the "design delay value on the delay fault defined signal path" and a "physical wiring area on the delay fault defined signal path" is used as <u>the predetermined delay value</u> ~~the weight~~.

10. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 3, wherein the product of the "design delay value on the delay fault defined signal path" and the sum of a "physical path area on the delay fault defined signal path" and an element area thereon is used as <u>the predetermined delay value</u> ~~the weight~~.

11. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 7, wherein a defect density is further used for multiplication as <u>the predetermined delay value</u> ~~the weight~~.

12. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 8, wherein a defect density is further used for multiplication as <u>the predetermined delay value</u> ~~the weight~~.

13. (Currently Amended)   A method of evaluating the quality of test sequences for

delay faults as claimed in claim 9, wherein a defect density is further used for multiplication as the predetermined delay value ~~the weight~~.

14. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 10, wherein a defect density is further used for multiplication as the predetermined delay value ~~the weight~~.

15. (Cancelled)

16. (Previously Presented)   A method of evaluating the quality of test sequences for delay faults having a step of generating test sequences for delay faults, wherein the "method of evaluating the quality of test sequences for delay faults" as claimed in claim 3 is applied to "test sequences for delay faults" generated in the step of generating test sequences for delay faults, to thereby calculate a fault coverage.

17. (Cancelled)

18. (Withdrawn)   A method of simulating the quality of test sequences for delay faults, wherein the "method of evaluating the quality of test sequences for delay faults" as claimed in claim 3 is applied to the given "test sequences for delay faults", to thereby calculate a fault coverage.

19. (Cancelled)

20. (Withdrawn)   A method of testing faults, wherein the "method of evaluating the quality of test sequences for delay faults" as claimed in claim 3 is applied to the "test sequences for delay faults" used for a test in testing steps of a semiconductor integrated circuit, to thereby calculate a fault coverage and determine whether the fault coverage satisfies a required value.

21. (Currently Amended)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 3, wherein a ratio of the "design delay value on the delay fault defined signal path" to the "timing design request value on the delay fault defined signal path" is used as the predetermined delay value the weight.

22. (Previously Presented)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 21, wherein the clock rate with respect to the delay fault defined signal path is used for the "timing design request value on the delay fault defined signal path".

23. (Previously Presented)   A method of evaluating the quality of test sequences for delay faults as claimed in claim 21, wherein when the delay fault defined signal path is a multicycle path, the product of the clock rate with respect to the delay fault defined signal path and the number of the multicycles is used for the "timing design request value on the delay fault defined signal path".